IN THE SPECIFICATION:

Please replace paragraph number **[0002]** with the following rewritten paragraph:

[0002] Field of the Invention: The present invention relates to an apparatus and a method for increasing semiconductor device density. In particular, the present invention relates to a method for producing vertically superimposed multi-chip devices usable with combined ~~flip-chip,~~ flip-chip, wire bond, and/or tape automated bonding ("TAB") assembly techniques to achieve densely packaged semiconductor devices.

Please replace paragraph number **[0012]** with the following rewritten paragraph:

[0012] State-of-the-art COB technology generally consists of three semiconductor ~~die-to-printed~~ die-to-printed circuit board conductive attachment techniques: flip-chip attachment, wirebonding, and TAB.

Please replace paragraph number **[0013]** with the following rewritten paragraph:

[0013] Flip-chip attachment consists of attaching a semiconductor die, generally having a BGA, a SLICC or a PGA, usually to a printed circuit board, although flip-chip attachment to leadframes is also known. With the BGA or SLICC, the solder or other conductive ball arrangement on the semiconductor die must be a mirror-image of the connecting bond pads on the printed circuit board such that a precise connection is made. The semiconductor die is bonded to the printed circuit board such as by refluxing the solder balls or curing the conductive polymer. With the PGA, the pin arrangement of the semiconductor die must be a mirror-image of the pin recesses on the printed circuit board. After insertion, the semiconductor die is generally bonded by soldering the pins into place. An under-fill encapsulant is generally disposed between the semiconductor die and the printed circuit board for environmental protection and to enhance the attachment of the die to the board. A variation of the pin-in-recess PGA is a J-lead PGA, wherein the loops of the ~~J's~~ Js are soldered to pads on the surface of the circuit board.

Please replace paragraph number **[0016]** with the following rewritten paragraph:

[0016] A so-called "leads over chip" (LOC) arrangement eliminates the die-attach paddle of the leadframe and supports the die by its active surface from the inner lead ends of the leadframe. This permits a wider variety of bond pad patterns on the die, extends the ~~leads-to-encapsulant~~ leads-to-encapsulant bond area and, with appropriate design parameters, can reduce the size of the packaged device for a given die size.

Please replace paragraph number **[0017]** with the following rewritten paragraph:

[0017] One method of increasing integrated circuit density is to stack dice vertically. U.S. Patent 5,012,323 issued April 30, 1991 to Farnworth teaches combining a pair of dice mounted on opposing sides of a leadframe. An upper, smaller die is back-bonded to the upper surface of the leads of the leadframe via a first adhesively coated, insulated film layer. A lower, larger die is face-bonded to the lower leadframe die-bonding region via a second, adhesively coated, insulative film layer. The wire-bonding pads on both upper ~~die and lower die~~ and lower dice are interconnected with the ends of their associated lead extensions with gold or aluminum bond wires. The lower die must be slightly larger than the upper die so that the die pads are accessible from above through a bonding window in the leadframe such that gold wire connections can be made to the lead extensions. This arrangement has a major disadvantage from a production standpoint, since the different size ~~die~~ dice require that different equipment produce the different dice or that the same equipment be switched over in different production runs to produce the different dice.

Please replace paragraph number **[0019]** with the following rewritten paragraph:

[0019] U.S. Patent 5,291,061 issued March 1, 1994 to Ball teaches a multiple stacked ~~dice~~ die device containing up to four stacked dice supported on a die-attach paddle of a leadframe, the assembly not exceeding the height of current single die packages, and wherein the bond pads of each die are wirebonded to lead fingers. The low profile of the device is achieved

by ~~close-tolerance~~ close-tolerance stacking which is made possible by a low-loop-profile wirebonding operation and thin adhesive layers between the stacked dice.

Please replace paragraph number **[0022]** with the following rewritten paragraph:

[0022] U.S. Patent 5,399,898 issued May 21, 1995 to Rostoker teaches multi-chip, multi-tier semiconductor arrangements based on single and double-sided flip-chips. Using these dice to form a stacked die package eliminates the need for wirebonding and thus reduces the size of the stacked ~~dice~~ die package. However, these die stacks require double-sided flip-chips which are expensive and difficult to manufacture.

Please replace paragraph number **[0027]** with the following rewritten paragraph:

[0027] Once the wafers are aligned and adhered, the wafer stack is mounted onto a stretchable adhesive film carried by a frame, as known in the art. The adhesive film is used to immobilize the wafer stack for scribing or sawing to singulate the dice or excise portions or segments of the wafers, sawing being highly preferred over scribing due to the double thickness of the ~~water~~ wafer stack. The wafer stack/film frame assembly is then sent through a dicing or singulation procedure wherein individual stacked dice pairs or wafer portions containing groups of dice pairs are cut from the wafer stack using a wafer dicing saw. The "streets" of the front and back wafers of the stack are, of course, aligned such that the circuitry on both wafers is not damaged during the dicing process.

Please replace paragraph number **[0029]** with the following rewritten paragraph:

[0029] After the paired dice or wafer portions are removed from the wafer stack and adhesive film frame by a pick-and-place apparatus as known in the art, the film being stretched to enhance separation of component parts of the wafer at the sawing, they may be attached to a carrier substrate, such as a ~~PCB~~ printed circuit board (PCB) or leadframe. A lower die of the dice pair is preferably configured as a flip-chip having, for example, BGA or SLICC solder bump connections, conductive polymer bumps, pin connections (PGA), or surface mount J-lead

connections extending substantially perpendicular from the circuitry face of the lower die for attachment and electrical communication of the die to the carrier substrate. The substrate is configured with a specific lead end or trace end pattern compatible with the specific pin out or bump connections on the lower die.

Please replace paragraph number **[0030]** with the following rewritten paragraph:

[0030] An upper die of the dice pair can be used to align the dice pair to the substrate. The use of the upper die for alignment allows the dice pair to be placed within plus or minus 0.0002-0.0003 inch of the desired location. Optical alignment ~~systems, including~~ systems including, without ~~limitation~~ limitation, pattern recognition systems as known in the art, are suitable to effect alignment to such tolerances. Once the dice pair is attached, an under-fill encapsulant is generally disposed between the lower die and the substrate (if other than a leadframe) for environmental protection and to enhance the attachment of the dice pair to the substrate.

Please replace paragraph number **[0031]** with the following rewritten paragraph:

[0031] Normally, the circuitry side or active surface of the upper die includes a plurality of bond pads. After attachment of the dice pair to the substrate, the bond pads of the upper die are brought into electrical communication with conductors of the substrate with wire bonds or TAB attachment. Bond wires and TAB traces of gold, aluminum or other suitable materials as known in the art are attached between the upper die bond pads and corresponding trace ends or lead ends of the substrate. If the die stack resides on a solid substrate such as a PCB, an encapsulant such as a glob-top is generally used to cover the bond wires or flex circuit to prevent contamination. If the die pair is secured to a leadframe, the assembly may be ~~plastic-encapsulated~~ plastic encapsulated as known in the art, as by transfer molding. Of course, preformed ceramic or metal packaging as known in the art may also be employed.

Please replace paragraph number **[0032]** with the following rewritten paragraph:

[0032] It is, of course, also understood that both the upper and lower dice may be ~~flip-chips~~ flip-chips having an array of minute solder balls or small pins for respective attachment to two opposing substrates such as facing ~~PCB's~~ PCBs or leadframes, or to a two-piece leadframe as known in the art.

Please replace paragraph number **[0041]** with the following rewritten paragraph:

[0041] FIG. 5 is a side ~~cross-sectional~~ cross-sectional view of the wafer pair along line 5-5 of FIG. 4;

Please replace paragraph number **[0048]** with the following rewritten paragraph:

[0048] Preferably, the upper wafer 202 and the lower wafer 204 contain complementary die locations, sizes, shapes and orientations such that when the wafers 202 and 204 are mounted, the dice of one wafer vertically align with that of the other. One technique for precisely aligning the wafers is to fabricate each wafer in such a manner that aligning the wafer ~~flats~~ flat lateral edges 106 (FIG. 1) automatically aligns the dice and circuitry. It is, of course, understood that the more complex techniques such as a pattern recognition system could be employed to precisely align the wafers.

Please replace paragraph number **[0050]** with the following rewritten paragraph:

[0050] FIG. 4 illustrates a top plan view of a partially kerfed or sawed wafer pair assembly 400. FIG. 5 illustrates a side ~~cross-sectional~~ cross-sectional view along line 5-5 of FIG. 4. Components common between FIGS. 1-5 retain the same numeric designation. The partially kerfed wafer pair assembly 400 shows the wafer pair 200 immobilized on the adhesive film 302 after a pass of a wafer dicing saw in one direction creating parallel kerfs 402. The wafer dicing saw is, per normal practice, preferably set to cut substantially through the wafer pair 200 without cutting the adhesive film ~~frame~~ 302 (see FIG. 5). If the dice 104 are to be singulated as dice pairs for use, the partially kerfed assembly 400 is rotated 90° and cut in the transverse

direction (see broken lines on FIG. 4) with parallel saw cuts, again as known in the art for cutting single wafers.

Please replace paragraph number **[0051]** with the following rewritten paragraph:

[0051] After the pairs of dice or wafer portions are cut and removed from the adhesive film by a pick-and-place apparatus or other known apparatus in the art, they may be attached to a substrate or printed circuit board. At least one side of the dice pair will preferably have an array of minute solder balls or other conductive elements (BGA or SLICC) or an array of small pins (PGA) disposed thereon for face-down attachment and electrical communication of the die to at least one substrate, again such as a PCB or leadframe.

Please replace paragraph number **[0058]** with the following rewritten paragraph:

[0058] FIG. 7 illustrates a side plan view of alternative die assembly 700 of the present invention. FIG. 7 shows a TAB attachment assembly rather than the wirebonding shown in FIG. 6. The alternate die assembly 700 is similar in structure to the die assembly 600 of FIG. 6; therefore, components common to both FIG. 6 and FIG. 7 retain the same numeric designation. A plurality of traces 704 on dielectric TAB ~~firms 702 are~~ films 702 is attached between the upper die bond pads 626 and corresponding trace or lead ends or other terminals 630 on the upper surface 614 of the substrate 606. It may be desirable to employ a heat sink member 912 between the ~~semiconductor substrates~~ upper die 602 and the lower die 604, either embedded in the adhesive or located between two adhesive layers, to promote heat transfer from the ~~semiconductor substrates~~ upper die 602 and the lower die 604.

Please replace paragraph number **[0060]** with the following rewritten paragraph:

[0060] FIG. 9 depicts yet another alternative embodiment 900 of the present invention comprising a die, partial wafer or wafer stack comprising first and second semiconductor substrates 902 and 904, each having bond pads 906 thereon communicating with integrated circuitry on each respective substrate. Unlike the previous embodiments of the invention,

semiconductor substrates 902 and 904 are stacked and adhered by adhesive 908 in active ~~face-to-back~~ face-to-back side relationships. Notches or recesses 910 or chamfers 911 at the semiconductor substrate peripheries expose bond pads 906 on lower substrate 904, of which there may be more than one to provide a three-or-more substrate stack. In accordance with the invention, it is preferred to practice this embodiment at the wafer level for ease of fabrication. It would be preferred to employ an insulating (dielectric) adhesive 908 between wafers in this embodiment, unless a very robust passivation layer is formed over the active surfaces of the lower wafer. Moreover, it may be desirable to employ a heat sink member 912 between the semiconductor substrates 902 and 904, either embedded in the adhesive or located between two adhesive layers, to promote heat transfer from the active surface of lower substrate 904 through an active or passive external cooling system as known in the art.

Please replace paragraph number **[0061]** with the following rewritten paragraph:

[0061] Having thus described in detail preferred embodiments of the present invention, it is to be understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof. For example, if the present invention is to be practiced at the wafer level, the integrated circuitry may be configured and fabricated for wafer-level operation with appropriate conductive traces and bond pad locations, as well as fuse and anti-fuse elements for removal of circuit segments proven defective during testing and ~~burn-in.~~ burn-in. Similarly, wafer portions or segments may be designed from the outset as discrete larger circuits, rather than as a plurality of linked discrete die. Again, such a configuration may be more economical of wafer real estate.